In the Specification

Page 1 - Insert after the title of the application - - This application is a division of application No. 10/449,426, filed May 30, 2003, which is now _____.. - -

In the Claims

Please cancel claims 1-13.

14. (Original) A method for detecting semiconductor process stress-induced defects comprising:

providing a test DRAM, said test DRAM comprising a transfer device having a channel region between first and second P+ regions formed in a N-well in a silicon substrate and a gate formed over said channel region, said second P+ region electrically connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing said test DRAM; and

monitoring said stressed test DRAM for spikes in first P+ region current during said stressing.

15. (Original) The method of claim 14, wherein said step of stressing comprises:

maintaining said test DRAM at an elevated temperature;

applying ground potential to said N-well and said first P+ region;

applying a voltage to said gate sufficient to turn on said transfer device; and

applying a reverse bias ramping voltage to said silicon substrate.

16. (Original) The method of claim 15, wherein said ground potential is zero volts and said ramping voltage is ramped from 0 to -6 volts and said elevated temperature is 100 to 200 °C..

17. (Original) A method for detecting semiconductor process stress-induced defects comprising:

providing a test DRAM, said test DRAM comprising a transfer device having a channel region between first and second P+ regions formed in a N-well in a silicon substrate and a gate formed over said channel region, said second P+ region electrically connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing said test DRAM; and

monitoring said stressed test DRAM for spikes in gate current during said stressing.

18. (Original) The method of claim 17, wherein said step of stressing comprises:

maintaining said test DRAM at an elevated temperature;

applying ground potential to said N-well, said silicon substrate and said gate; and

applying a reverse bias ramping voltage to said first P+ region.

19. (Original) The method of claim 18, wherein said ground potential is zero volts and said ramping voltage is ramped from 0 to -6 volts and said elevated temperature is 100 to 200 °C.

20. (Original) A method for detecting semiconductor process stress-induced defects comprising:

providing a test DRAM, said test DRAM comprising a transfer device comprising a channel region between first and second P+ regions formed in a N-well in a silicon substrate and a gate formed over said channel region, said second P+ region electrically

connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing said test DRAM;

measuring during said stressing, for said test DRAM, the current through said first P+ region as a function of a forward bias voltage applied between said first P+ region and said N-well at at least a pre-selected forward bias voltage; and

determining the frequency distribution of the slope of said forward bias voltage versus said first P+ region current at said pre-selected forward bias voltage for said one or more test DRAMs.

21. (Original) The method of claim 20, wherein said step of stressing comprises:

applying ground potential to said N-well and said silicon substrate;

applying a voltage to said gate sufficient to turn off said transfer device; and

applying a forward bias ramping voltage between said first P+ region and said N-well.

22. (Original) The method of claim 21, wherein said ground potential is zero volts and said ramping voltage is ramped from 0 to 0.85 and said pre-selected voltage is between 0.4 and 0.5 volts.

23. (Original) The method of claim 20 further comprising:

providing one or more reference devices, said reference devices each comprising a third P+ region formed in a N-well in said silicon substrate, said P+ region electrically connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing each said reference device identically to said test DRAM;

measuring during said stressing, for each said reference device, the current through said third P+ region as a function of said forward bias voltage applied between said third P+ region and said N-well at at least said predetermined forward bias voltage;

determining the frequency distribution of the slope of said forward bias voltage versus said P+ region current at said pre-selected forward bias voltage for said one or more of reference devices; and

comparing said frequency distribution obtained from said reference devices to said frequency distribution obtained from said test DRAMs.

24. (Original) A method for detecting semiconductor process stress-induced defects comprising:

providing a test DRAM, said test DRAM comprising a transfer device comprising a channel region between first and second P+ regions formed in a N-well in a silicon substrate and a gate formed over said channel region, said second P+ region electrically connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing said test DRAM for a pre-determined amount of time; and

monitoring, after said stressing, each said test DRAM for soft breakdown.

25. (Original) The method of claim 24, wherein said step of stressing comprises:

maintaining said test DRAM at an elevated temperature;

applying ground potential to said first P+ region and said N-well;

applying a voltage to said gate sufficient to turn on said transfer device; and

applying a fixed reverse bias voltage to said silicon substrate; and

wherein said monitoring includes measuring a current through said first P+ diffusion as a function of time.

26. (Original) The method of claim 25, wherein said ground potential is zero volts, said fixed voltage is between-6.3 and 0 volts, said fixed time is 0.5 hours or more and said elevated temperature is 100 to 200 °C.

27. (Original) The method of claim 24, wherein said step of stressing comprises:

maintaining said test DRAM at an elevated temperature;

applying ground potential to said N-well, said gate and said substrate;

applying a fixed reverse bias voltage to said first P+ region; and

wherein said monitoring includes measuring a current through said gate as a function of time.

28. (Original) The method of claim 27, wherein said ground potential is zero volts, said fixed voltage is between-6.3 and less than 0 volts, said fixed time is 0.5 hours or more and said elevated temperature is 100 to 200 °C.

29. (Original) A method of fabricating an antifuse comprising:

providing a silicon substrate having a surface;

forming a ring of shallow trench isolation having an inner and an outer perimeter in said substrate extending from said surface of said substrate into said substrate;

forming a polysilicon gate overlapping said inner perimeter of said shallow trench isolation on said surface of said substrate, said polysilicon gate comprising a dielectric layer between said surface of said substrate and a polysilicon layer, said polysilicon gate having an inner and outer perimeter;

damaging said dielectric layer in a region along said inner perimeter of said polysilicon gate with a heavy ion specie implant to lower the breakdown voltage of said damaged dielectric layer in said region compared to the breakdown voltage in undamaged dielectric regions; and

forming a diffused region in said silicon substrate within the inner perimeter of said shallow trench isolation, said diffused region extending from said surface of said substrate into said substrate a depth not exceeding a depth of said shallow trench isolation.

30. (Original) The method of claim 29 wherein:

said diffused region has a length of 1 to 100 microns and a width of 1 to 10 microns;

said polysilicon gate has a width of 0.5 to 1.5 microns; and

said polysilicon gate overlaps said diffused region by 0.1 to 0.6 microns.

31. (Original) The method of claim 29 wherein said heavy ion specie is selected from the group consisting of germanium ion and arsenic ion.

32. (Original) The method of claim 29 further comprising forming a diffused-well of opposite polarity doping from said diffused region.

Cancel claims 33-40.

The Examiner is urged to call the undersigned at the number show below if, in the Examiner's opinion, further aid is needed in the prosecution of this application.

Any fees required for entering this amendment should be charged to our deposit account, Number 09-0456.

Respectfully submitted,

12/9/03

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